REMARKS

Objection to Drawings

Figures 1A-1E were objected to because they are not designated by a legend such as "Prior Art".

Figures 1A-1E, however, do not simply illustrate old art. Figures 1A-1E also illustrate the mechanism which the inventor of the present invention made clear for the first time, for the generation of the residues during the steps of fabricating a gate electrode. Therefore, it is inappropriate and unnecessary to attach a legend such as "Prior Art" to Figures 1A-1E.

Rejections under 35 USC §102(e)

Claims 1-4, 11-12 and 19-20 were rejected under 35 USC §102(e) as being anticipated by Joo et al (U.S. Patent No. 6,627,494).

The Examiner alleged that all the steps in the invention according to claims 1 and 2 are disclosed in Joo et al. However, the present invention is clearly different from Joo et al, especially in the step of forming the oxide film on the surface with the natural oxide film removed as described in detail below.

In Joo et al, a TaON film 5 is deposited by chemical vapor deposition on the surface of a conductive film 4 of a doped polysilicon with the natural oxide film removed.

On the other hand, claims 1 and 2 recite, among other things, "oxidizing the surface of the film with the natural oxide film removed to form an oxide film which is homogeneous in comparison with the natural oxide film." Thus, according to the present invention, the surface of

the film containing silicon with the natural oxide film removed is oxidized to form an oxide film which is homogeneous in comparison with the natural oxide film. Joo et al does not teach or suggest "oxidizing the surface of the film with the natural oxide film removed to form an oxide film which is homogeneous in comparison with the natural oxide film," as recited in amended claims 1 and 2.

For at least these reasons, claims 1 and 2 patentably distinguish over Joo et al. Claims 3, 4, 11-12 and 19-20, depending from claim 1 or 2, also patentably distinguish over Joo et al for at least the same reasons.

Claim 17 was rejected under 35 U.S.C. 1O2(e) as being anticipated by Lee et at. (IEEE 1997 Symposium on VLSI Technology Digest of Technical Papers, pp.131-132).

Claim 17, as amended, recites, among other things, "the surface of the film being kept without being exposed to the atmosphere for the duration from the step of forming the film to the step of forming the mask." Thus, according to claim 17, the surface of the film containing a silicon is kept without being exposed to the atmosphere for the duration from the step of forming the film to the step of forming the mask. Claim 17 is directed to the second embodiment. The surface of the film containing silicon below the mask is prevented from being exposed to the atmosphere during the intervals of the steps.

Lee et al discusses fabrication of 0.06 μm poly-Si gate using DUV lithography with a designed $Si_xO_yN_z$ film as an ARC and hard mask and discloses that the mask ($Si_xO_yN_z$) stack is

deposited in a commercial P5000 PECVI) chamber. Lee et at simply forms a $Si_xO_yN_z$ film and has nothing to do with the handling of a film surface on which an oxide film is to be formed.

Accordingly, Lee et al does not teach or suggest, among other things, "the surface of the film being kept without being exposed to the atmosphere for the duration from the step of forming the film to the step of forming the mask," as recited in claim 17.

For at least these reasons, claim 17 patentably distinguishes over Lee et al.

Rejections under 35 USC §103(a)

Claims 5-8 were rejected under 35 USC §103(a) as being obvious over Joo et al (U.S. Patent No. 6,627,494), in view of Houng et al (U.S. Patent No. 6,689,645).

Claims 5-8 directly or indirectly depend from claims 1 or 2. Houng et al has been cited for allegedly disclosing the step of cleaning the surface of silicon-containing film to remove native oxide and then oxidizing the native-oxide-free surface of the film with HPM to form an oxide layer on the film. The Examiner alleged that it would have been obvious to one having ordinary skill in the art to use the method of forming the oxide layer by oxidization as taught by Houng et al in Joo et al if the oxide film in Joo et al is silicon oxide instead of TaON.

However, in Joo et al, a TaON film is formed by LPCVD on a conductive film to be a floating gate and the TaON film is clearly different from an oxide film formed on a surface of a conductive film by oxidizing the surface of the conductive film.

In contrast, according to the present invention, the oxide film which is homogeneous compared with the natural oxide film is formed by oxidizing the surface of the film containing

silicon with the natural oxide film removed. In this way, the residues of the film containing silicon in the region other than the region for a gate electrode to be formed can be suppressed. According to the present invention, the inhomogeneous natural oxide film formed on the film to be a gate electrode is replaced with the homogeneous oxide film formed by oxidizing the surface of the film to be a gate electrode with a prescribed method prior to patterning the gate electrode.

It is the present inventors who first clarified the mechanism for the generation of the residues during the patterning of gate electrodes. Without such knowledge of the mechanism, the present invention would not be reached by a person of ordinary skill in the art. The mechanism for the generation of the residues is disclosed in detail in the explanation of the present invention in the specification.

Joo et al simply discloses that the TaON film is formed on the conductive film by vapor deposition. Joo et al does not teach or suggest the mechanism for the generation of the residues during the patterning of gate electrodes. Accordingly, it would almost be impossible to use the method of forming the oxide film by the oxidization with a chemical liquid in Joo et al instead of forming the TaON film without the knowledge regarding the generation of the residues during the patterning of gate electrodes.

Moreover, the oxide film in the present invention is used in forming a semiconductor device with a gate electrode and does not constitute a part of the semiconductor device itself. On the other hand, the TaON film in Joo et al constitutes a part of a semiconductor device with a floating gate and a control gate. Namely, the TaON film is a gate insulation film between the

floating gate and the control gate. Thus, the oxide film disclosed in Joo et al has nothing to do with the present invention.

Accordingly, even if Joo et al discloses the TaON film and Houng et al discloses the method of forming an oxide film with chemical liquids, a person of ordinary skill in the art would not have been motivated to reach the present invention as amended claims 1 and 2 and claims 5-8.

For at least these reasons, claims 5-8 patentably distinguish over Joo et al and Houng et al.

Claims 9-10, 13-16 and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al. (US.P. 6,627, 494).

As discussed above, amended claims 1 and 2 patentably distinguish over Joo et al. Claims 9, 10 and 13-16, directly or indirectly depending from claim 1 or 2, also patentably distinguish over Joo et al for at least the same reasons.

Amended claim 18 recites "the surface of the film being kept without being exposed to the atmosphere for the duration from the step of forming the film to the step of forming the oxide film." Thus, the surface of the film containing a silicon is kept without being exposed to the atmosphere for the duration from the step of forming the film to the step of forming the oxide film, which is disclosed in the second embodiment of the present invention. Joo et al does not teach or suggest such a technical feature.

For at least these reasons, claim 18 patentably distinguishes over Joo et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Sadao Kinashi
Attorney for Applicants
Registration No. 48,075
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

SK/sg/jl